

AD-A097 279

ILLINOIS UNIV AT URBANA COORDINATED SCIENCE LAB

F/G 17/9

NEW TECHNIQUES IN DIGITAL SIGNAL PROCESSING FOR SYNTHETIC APERT--ETC(U)

FEB 81 W K JENKINS

AFOSR-79-0029

UNCLASSIFIED

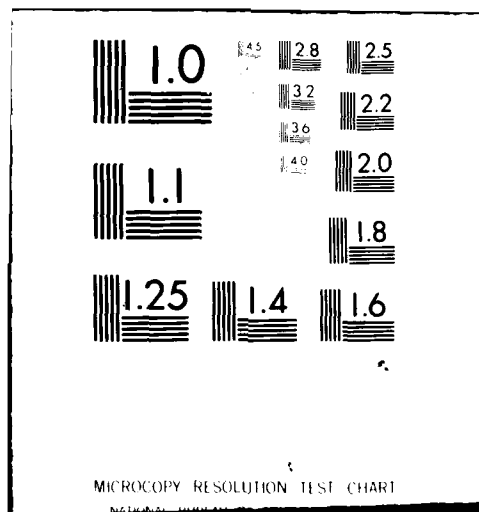
AFOSR-TR-81-0321

NL

1 1P 1
ADA
C 97-9



END
DATE
FILMED
5-81
DTIC



UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

(2)

LEVEL II

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER 18 AFOSR-TR-81-0321	2. GOVT ACCESSION NO. AD-A097279	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) NEW TECHNIQUES IN DIGITAL SIGNAL PROCESSING FOR SYNTHETIC APERTURE RADAR		5. TYPE OF REPORT & PERIOD COVERED FINAL, 1 Jan 79 - 31 Dec 80
7. AUTHOR(s) W.K. Jenkins		6. PERFORMING ORG. REPORT NUMBER
9. PERFORMING ORGANIZATION NAME AND ADDRESS Department of Electrical Engineering and the Coordinated Science Laboratory, University of Illinois, Urbana-Champaign IL 61801		8. CONTRACT OR GRANT NUMBER(s) AFOSR-79-0029
12. CONTROLLING OFFICE NAME AND ADDRESS Air Force Office of Scientific Research/NM Bolling AFB DC 20332		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 2304/A6 61102F A6
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office) (9) Final Rept. 1 Jan 79-31 Dec 80		11. REPORT DATE February 1981
		12. NUMBER OF PAGES 12
		13. SECURITY CLASS. (of this report) Unclassified
16. DISTRIBUTION STATEMENT (of this Report) Approved for public release; distribution unlimited.		15. DECLASSIFICATION/DOWNGRADING SCHEDULE
17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)		
18. SUPPLEMENTARY NOTES		
19. KEY WORDS (Continue on reverse side if necessary and identify by block number)		
20. ABSTRACT (Continue on reverse side if necessary and identify by block number) Research supported by this grant has been concentrated in four distinct, but related projects: 1) an analysis of inherent phase distortion in rectangular and polar format FFT processing algorithms, 2) a SAR computer simulation with polar format recording, 3) a study of 2D interpolators for polar-to-rectangular coordinate transformation, and 4) an investigation of number theoretic concepts for high speed failure resistant digital processors required in real-time SAR systems.		

AD-A097279

DTIC
ELECTE
APR 2 1981
B

DTIC FILE COPY

DD FORM 1 JAN 73 1473

UNCLASSIFIED 097700
SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

Copy 1 AFOSR-TR- 81 - 0321

Research Summary

"New Techniques in Digital Signal Processing
for Synthetic Aperture Radar"

Grant AFOSR-79-0029
January 1, 1979 - December 31, 1980

W. K. Jenkins, Principal Investigator
Department of Electrical Engineering and
The Coordinated Science Laboratory
University of Illinois
Urbana-Champaign, IL 61801

FINAL REPORT
February 1981

Approved for public release:
distribution unlimited.

81 4 2 036

Contents

	Page
1. Summary of Research on Grant AFOSR-79-0029	1
1.1 Analysis of Inherent Phase Distortion	1
1.2 SAR Computer Simulations	2
1.3 Two-Dimensional Interpolators	6
1.4 Residue Number Concepts for Digital Processors	6
2. Future Directions	8
3. Publications Supported by or Relating to Grant AFOSR-79-0029	9
4. Related Research Grants and Submitted Proposals	12

Approved For	<input checked="" type="checkbox"/>
1.11.1.1	<input type="checkbox"/>
1.11.1.2	<input type="checkbox"/>
1.11.1.3	<input type="checkbox"/>
1.11.1.4	<input type="checkbox"/>
1.11.1.5	<input type="checkbox"/>
1.11.1.6	<input type="checkbox"/>
1.11.1.7	<input type="checkbox"/>
1.11.1.8	<input type="checkbox"/>
1.11.1.9	<input type="checkbox"/>
1.11.1.10	<input type="checkbox"/>
1.11.1.11	<input type="checkbox"/>
1.11.1.12	<input type="checkbox"/>
1.11.1.13	<input type="checkbox"/>
1.11.1.14	<input type="checkbox"/>
1.11.1.15	<input type="checkbox"/>
1.11.1.16	<input type="checkbox"/>
1.11.1.17	<input type="checkbox"/>
1.11.1.18	<input type="checkbox"/>
1.11.1.19	<input type="checkbox"/>
1.11.1.20	<input type="checkbox"/>
1.11.1.21	<input type="checkbox"/>
1.11.1.22	<input type="checkbox"/>
1.11.1.23	<input type="checkbox"/>
1.11.1.24	<input type="checkbox"/>
1.11.1.25	<input type="checkbox"/>
1.11.1.26	<input type="checkbox"/>
1.11.1.27	<input type="checkbox"/>
1.11.1.28	<input type="checkbox"/>
1.11.1.29	<input type="checkbox"/>
1.11.1.30	<input type="checkbox"/>
1.11.1.31	<input type="checkbox"/>
1.11.1.32	<input type="checkbox"/>
1.11.1.33	<input type="checkbox"/>
1.11.1.34	<input type="checkbox"/>
1.11.1.35	<input type="checkbox"/>
1.11.1.36	<input type="checkbox"/>
1.11.1.37	<input type="checkbox"/>
1.11.1.38	<input type="checkbox"/>
1.11.1.39	<input type="checkbox"/>
1.11.1.40	<input type="checkbox"/>
1.11.1.41	<input type="checkbox"/>
1.11.1.42	<input type="checkbox"/>
1.11.1.43	<input type="checkbox"/>
1.11.1.44	<input type="checkbox"/>
1.11.1.45	<input type="checkbox"/>
1.11.1.46	<input type="checkbox"/>
1.11.1.47	<input type="checkbox"/>
1.11.1.48	<input type="checkbox"/>
1.11.1.49	<input type="checkbox"/>
1.11.1.50	<input type="checkbox"/>
1.11.1.51	<input type="checkbox"/>
1.11.1.52	<input type="checkbox"/>
1.11.1.53	<input type="checkbox"/>
1.11.1.54	<input type="checkbox"/>
1.11.1.55	<input type="checkbox"/>
1.11.1.56	<input type="checkbox"/>
1.11.1.57	<input type="checkbox"/>
1.11.1.58	<input type="checkbox"/>
1.11.1.59	<input type="checkbox"/>
1.11.1.60	<input type="checkbox"/>
1.11.1.61	<input type="checkbox"/>
1.11.1.62	<input type="checkbox"/>
1.11.1.63	<input type="checkbox"/>
1.11.1.64	<input type="checkbox"/>
1.11.1.65	<input type="checkbox"/>
1.11.1.66	<input type="checkbox"/>
1.11.1.67	<input type="checkbox"/>
1.11.1.68	<input type="checkbox"/>
1.11.1.69	<input type="checkbox"/>
1.11.1.70	<input type="checkbox"/>
1.11.1.71	<input type="checkbox"/>
1.11.1.72	<input type="checkbox"/>
1.11.1.73	<input type="checkbox"/>
1.11.1.74	<input type="checkbox"/>
1.11.1.75	<input type="checkbox"/>
1.11.1.76	<input type="checkbox"/>
1.11.1.77	<input type="checkbox"/>
1.11.1.78	<input type="checkbox"/>
1.11.1.79	<input type="checkbox"/>
1.11.1.80	<input type="checkbox"/>
1.11.1.81	<input type="checkbox"/>
1.11.1.82	<input type="checkbox"/>
1.11.1.83	<input type="checkbox"/>
1.11.1.84	<input type="checkbox"/>
1.11.1.85	<input type="checkbox"/>
1.11.1.86	<input type="checkbox"/>
1.11.1.87	<input type="checkbox"/>
1.11.1.88	<input type="checkbox"/>
1.11.1.89	<input type="checkbox"/>
1.11.1.90	<input type="checkbox"/>
1.11.1.91	<input type="checkbox"/>
1.11.1.92	<input type="checkbox"/>
1.11.1.93	<input type="checkbox"/>
1.11.1.94	<input type="checkbox"/>
1.11.1.95	<input type="checkbox"/>
1.11.1.96	<input type="checkbox"/>
1.11.1.97	<input type="checkbox"/>
1.11.1.98	<input type="checkbox"/>
1.11.1.99	<input type="checkbox"/>
1.11.1.100	<input type="checkbox"/>
1.11.1.101	<input type="checkbox"/>
1.11.1.102	<input type="checkbox"/>
1.11.1.103	<input type="checkbox"/>
1.11.1.104	<input type="checkbox"/>
1.11.1.105	<input type="checkbox"/>
1.11.1.106	<input type="checkbox"/>
1.11.1.107	<input type="checkbox"/>
1.11.1.108	<input type="checkbox"/>
1.11.1.109	<input type="checkbox"/>
1.11.1.110	<input type="checkbox"/>
1.11.1.111	<input type="checkbox"/>
1.11.1.112	<input type="checkbox"/>
1.11.1.113	<input type="checkbox"/>
1.11.1.114	<input type="checkbox"/>
1.11.1.115	<input type="checkbox"/>
1.11.1.116	<input type="checkbox"/>
1.11.1.117	<input type="checkbox"/>
1.11.1.118	<input type="checkbox"/>
1.11.1.119	<input type="checkbox"/>
1.11.1.120	<input type="checkbox"/>
1.11.1.121	<input type="checkbox"/>
1.11.1.122	<input type="checkbox"/>
1.11.1.123	<input type="checkbox"/>
1.11.1.124	<input type="checkbox"/>
1.11.1.125	<input type="checkbox"/>
1.11.1.126	<input type="checkbox"/>
1.11.1.127	<input type="checkbox"/>
1.11.1.128	<input type="checkbox"/>
1.11.1.129	<input type="checkbox"/>
1.11.1.130	<input type="checkbox"/>
1.11.1.131	<input type="checkbox"/>
1.11.1.132	<input type="checkbox"/>
1.11.1.133	<input type="checkbox"/>
1.11.1.134	<input type="checkbox"/>
1.11.1.135	<input type="checkbox"/>
1.11.1.136	<input type="checkbox"/>
1.11.1.137	<input type="checkbox"/>
1.11.1.138	<input type="checkbox"/>
1.11.1.139	<input type="checkbox"/>
1.11.1.140	<input type="checkbox"/>
1.11.1.141	<input type="checkbox"/>
1.11.1.142	<input type="checkbox"/>
1.11.1.143	<input type="checkbox"/>
1.11.1.144	<input type="checkbox"/>
1.11.1.145	<input type="checkbox"/>
1.11.1.146	<input type="checkbox"/>
1.11.1.147	<input type="checkbox"/>
1.11.1.148	<input type="checkbox"/>
1.11.1.149	<input type="checkbox"/>
1.11.1.150	<input type="checkbox"/>
1.11.1.151	<input type="checkbox"/>
1.11.1.152	<input type="checkbox"/>
1.11.1.153	<input type="checkbox"/>
1.11.1.154	<input type="checkbox"/>
1.11.1.155	<input type="checkbox"/>
1.11.1.156	<input type="checkbox"/>
1.11.1.157	<input type="checkbox"/>
1.11.1.158	<input type="checkbox"/>
1.11.1.159	<input type="checkbox"/>
1.11.1.160	<input type="checkbox"/>
1.11.1.161	<input type="checkbox"/>
1.11.1.162	<input type="checkbox"/>
1.11.1.163	<input type="checkbox"/>
1.11.1.164	<input type="checkbox"/>
1.11.1.165	<input type="checkbox"/>
1.11.1.166	<input type="checkbox"/>
1.11.1.167	<input type="checkbox"/>
1.11.1.168	<input type="checkbox"/>
1.11.1.169	<input type="checkbox"/>
1.11.1.170	<input type="checkbox"/>
1.11.1.171	<input type="checkbox"/>
1.11.1.172	<input type="checkbox"/>
1.11.1.173	<input type="checkbox"/>
1.11.1.174	<input type="checkbox"/>
1.11.1.175	<input type="checkbox"/>
1.11.1.176	<input type="checkbox"/>
1.11.1.177	<input type="checkbox"/>
1.11.1.178	<input type="checkbox"/>
1.11.1.179	<input type="checkbox"/>
1.11.1.180	<input type="checkbox"/>
1.11.1.181	<input type="checkbox"/>
1.11.1.182	<input type="checkbox"/>
1.11.1.183	<input type="checkbox"/>
1.11.1.184	<input type="checkbox"/>
1.11.1.185	<input type="checkbox"/>
1.11.1.186	<input type="checkbox"/>
1.11.1.187	<input type="checkbox"/>
1.11.1.188	<input type="checkbox"/>
1.11.1.189	<input type="checkbox"/>
1.11.1.190	<input type="checkbox"/>
1.11.1.191	<input type="checkbox"/>
1.11.1.192	<input type="checkbox"/>
1.11.1.193	<input type="checkbox"/>
1.11.1.194	<input type="checkbox"/>
1.11.1.195	<input type="checkbox"/>
1.11.1.196	<input type="checkbox"/>
1.11.1.197	<input type="checkbox"/>
1.11.1.198	<input type="checkbox"/>
1.11.1.199	<input type="checkbox"/>
1.11.1.200	<input type="checkbox"/>
1.11.1.201	<input type="checkbox"/>
1.11.1.202	<input type="checkbox"/>
1.11.1.203	<input type="checkbox"/>
1.11.1.204	<input type="checkbox"/>
1.11.1.205	<input type="checkbox"/>
1.11.1.206	<input type="checkbox"/>
1.11.1.207	<input type="checkbox"/>
1.11.1.208	<input type="checkbox"/>
1.11.1.209	<input type="checkbox"/>
1.11.1.210	<input type="checkbox"/>
1.11.1.211	<input type="checkbox"/>
1.11.1.212	<input type="checkbox"/>
1.11.1.213	<input type="checkbox"/>
1.11.1.214	<input type="checkbox"/>
1.11.1.215	<input type="checkbox"/>
1.11.1.216	<input type="checkbox"/>
1.11.1.217	<input type="checkbox"/>
1.11.1.218	<input type="checkbox"/>
1.11.1.219	<input type="checkbox"/>
1.11.1.220	<input type="checkbox"/>
1.11.1.221	<input type="checkbox"/>
1.11.1.222	<input type="checkbox"/>
1.11.1.223	<input type="checkbox"/>
1.11.1.224	<input type="checkbox"/>
1.11.1.225	<input type="checkbox"/>
1.11.1.226	<input type="checkbox"/>
1.11.1.227	<input type="checkbox"/>
1.11.1.228	<input type="checkbox"/>
1.11.1.229	<input type="checkbox"/>
1.11.1.230	<input type="checkbox"/>
1.11.1.231	<input type="checkbox"/>
1.11.1.232	<input type="checkbox"/>
1.11.1.233	<input type="checkbox"/>
1.11.1.234	<input type="checkbox"/>
1.11.1.235	<input type="checkbox"/>
1.11.1.236	<input type="checkbox"/>
1.11.1.237	<input type="checkbox"/>
1.11.1.238	<input type="checkbox"/>
1.11.1.239	<input type="checkbox"/>
1.11.1.240	<input type="checkbox"/>
1.11.1.241	<input type="checkbox"/>
1.11.1.242	<input type="checkbox"/>
1.11.1.243	<input type="checkbox"/>
1.11.1.244	<input type="checkbox"/>
1.11.1.245	<input type="checkbox"/>
1.11.1.246	<input type="checkbox"/>
1.11.1.247	<input type="checkbox"/>
1.11.1.248	<input type="checkbox"/>
1.11.1.249	<input type="checkbox"/>
1.11.1.250	<input type="checkbox"/>
1.11.1.251	<input type="checkbox"/>
1.11.1.252	<input type="checkbox"/>
1.11.1.253	<input type="checkbox"/>
1.11.1.254	<input type="checkbox"/>
1.11.1.255	<input type="checkbox"/>
1.11.1.256	<input type="checkbox"/>
1.11.1.257	<input type="checkbox"/>
1.11.1.258	<input type="checkbox"/>
1.11.1.259	<input type="checkbox"/>
1.11.1.260	<input type="checkbox"/>
1.11.1.261	<input type="checkbox"/>
1.11.1.262	<input type="checkbox"/>
1.11.1.263	<input type="checkbox"/>
1.11.1.264	<input type="checkbox"/>
1.11.1.265	<input type="checkbox"/>
1.11.1.266	<input type="checkbox"/>
1.11.1.267	<input type="checkbox"/>
1.11.1.268	<input type="checkbox"/>
1.11.1.269	<input type="checkbox"/>
1.11.1.270	<input type="checkbox"/>
1.11.1.271	<input type="checkbox"/>
1.11.1.272	<input type="checkbox"/>
1.11.1.273	<input type="checkbox"/>
1.11.1.274	<input type="checkbox"/>
1.11.1.275	<input type="checkbox"/>
1.11.1.276	<input type="checkbox"/>
1.11.1.277	<input type="checkbox"/>
1.11.1.278	<input type="checkbox"/>
1.11.1.279	<input type="checkbox"/>
1.11.1.280	<input type="checkbox"/>
1.11.1.281	<input type="checkbox"/>
1.11.1.282	<input type="checkbox"/>
1.11.1.283	<input type="checkbox"/>
1.11.1.284	<input type="checkbox"/>
1.11.1.285	<input type="checkbox"/>
1.11.1.286	<input type="checkbox"/>
1.11.1.287	<input type="checkbox"/>
1.11.1.288	<input type="checkbox"/>
1.11.1.289	<input type="checkbox"/>
1.11.1.290	<input type="checkbox"/>
1.11.1.291	<input type="checkbox"/>
1.11.1.292	<input type="checkbox"/>
1.11.1.293	<input type="checkbox"/>
1.11.1.294	<input type="checkbox"/>
1.11.1.295	<input type="checkbox"/>
1.11.1.296	<input type="checkbox"/>
1.11.1.297	<input type="checkbox"/>
1.11.1.298	<input type="checkbox"/>
1.11.1.299	<input type="checkbox"/>
1.11.1.300	<input type="checkbox"/>
1.11.1.301	<input type="checkbox"/>
1.11.1.302	<input type="checkbox"/>
1.11.1.303	<input type="checkbox"/>
1.11.1.304	<input type="checkbox"/>
1.11.1.305	<input type="checkbox"/>
1.11.1.306	<input type="checkbox"/>
1.11.1.307	<input type="checkbox"/>
1.11.1.308	<input type="checkbox"/>
1.11.1.309	<input type="checkbox"/>
1.11.1.310	<input type="checkbox"/>
1.11.1.311	<input type="checkbox"/>
1.11.1.312	<input type="checkbox"/>
1.11.1.313	<input type="checkbox"/>
1.11.1.314	<input type="checkbox"/>
1.11.1.315	<input type="checkbox"/>
1.11.1.316	<input type="checkbox"/>
1.11.1.317	<input type="checkbox"/>
1.11.1.318	<input type="checkbox"/>
1.11.1.319	<input type="checkbox"/>
1.11.1.320	<input type="checkbox"/>
1.11.1.321	<input type="checkbox"/>
1.11.1.322	<input type="checkbox"/>
1.11.1.323	<input type="checkbox"/>
1.11.1.324	<input type="checkbox"/>
1.11.1.325	<input type="checkbox"/>
1.11.1.326	<input type="checkbox"/>
1.11.1.327	<input type="checkbox"/>
1.11.1.328	<input type="checkbox"/>
1.11.1.329	<input type="checkbox"/>
1.11.1.330	<input type="checkbox"/>
1.11.1.331	<input type="checkbox"/>
1.11.1.332	<input type="checkbox"/>
1.11.1.333	<input type="checkbox"/>
1.11.1.334	<input type="checkbox"/>
1.11.1.335	<input type="checkbox"/>
1.11.1.336	<input type="checkbox"/>
1.11.1.337	<input type="checkbox"/>
1.11.1.338	<input type="checkbox"/>
1.11.1.339	<input type="checkbox"/>
1.11.1.340	<input type="checkbox"/>
1.11.1.341	<input type="checkbox"/>
1.11.1.342	<input type="checkbox"/>
1.11.1.343	<input type="checkbox"/>
1.11.1.344	<input type="checkbox"/>
1.11.1.345	<input type="checkbox"/>
1.11.1.346	<input type="checkbox"/>
1.11.1.347	<input type="checkbox"/>
1.11.1.348	<input type="checkbox"/>
1.11.1.349	<input type="checkbox"/>
1.11.1.350	<input type="checkbox"/>
1.11.1.351	<input type="checkbox"/>
1.11.1.352	<input type="checkbox"/>
1.11.1.353	<input type="checkbox"/>
1.11.1.354	<input type="checkbox"/>
1.11.1.355	<input type="checkbox"/>
1.11.1.356	<input type="checkbox"/>
1.11.1.357	<input type="checkbox"/>
1.11.1.358	<input type="checkbox"/>
1.11.1.359	<input type="checkbox"/>
1.11.1.360	<input type="checkbox"/>
1.11.1.361	<input type="checkbox"/>
1.11.1.362	<input type="checkbox"/>
1.11.1.363	<input type="checkbox"/>
1.11.1.364	<input type="checkbox"/>
1.11.1.365	

1. Summary of Research on Grant AFOSR-79-0029

Research supported by this grant has been concentrated in four distinct, but related projects: 1) an analysis of inherent phase distortion in rectangular and polar format FFT processing algorithms, 2) a SAR computer simulation with polar format recording, 3) a study of 2D interpolators for polar-to-rectangular coordinate transformation, and 4) an investigation of number theoretic concepts for high speed failure resistant digital processors required in real-time SAR systems. The following paragraphs summarize results in these four areas.

1.1 Analysis of Inherent Phase Distortion

Our study of SAR signal processing algorithms began with an analytical evaluation of inherent phase errors that occur in "stretch" processing that is popular in present day spotlight mode SARs. In stretch systems, linear FM waveforms are transmitted at N distinct positions along the flight path, at which points the returns are received, demodulated, sampled, and recorded for subsequent processing. This creates a linear FM variation in each return from a point target along the range coordinate (time). The relative motion of the radar and the ground creates an approximate linear FM variation in point target responses along the azimuthal coordinate (direction of flight), due to the Doppler effect. After the data have been recorded at all N positions, a reference function is mixed with the data to focus a predetermined reference target, and the ensemble is processed with a 2D FFT to resolve the targets by spectral analysis. Stretch processing is motivated by the computational efficiency of the FFT, which holds potential for real-time processing.

Unfortunately, there are two serious deficiencies in stretch signal processing. The first is that the azimuthal frequency variation is only approximately linear FM, so that there are residual phase errors which depend on target position, and which cannot be corrected by the FFT algorithm. The second is that targets move in range relative to the radar, so that polar format recording is required for spotlight mode operation. Since the FFT requires data samples in a rectangular coordinate system, 2D interpolation is needed to generate data samples which lie on a rectangular raster. The 2D interpolation requires considerable computation, to the extent that it may be a dominant factor in the overall computational complexity of the stretch algorithm.

In our study of phase error effects, analytical expressions were derived for the phase of the recorded response from point targets in the ground plane. Phase functions were derived for both polar and rectangular recording systems. Since the phase response is a relatively complicated nonlinear function of target position, it was expanded in a Taylor series so the effects of linear phase error, quadratic phase error, and higher order phase error terms could be identified. The results of this analysis isolate the effects of linear phase error (misregistration) and quadratic phase error (defocus) in both the polar and rectangular domains [20].

In an independent analysis, residual phase errors were analyzed for an algorithm which uses FFT stretch processing in the azimuthal coordinate only, assuming that range processing is implemented independently, possibly by real-time analog devices. The results of this analysis are useful for relating phase error to image size for systems using hybrid signal processing concepts [17].

1.2 SAR Computer Simulations

A SAR computer simulation was developed that processes recorded data files to simulate system response to ideal point targets. Artificial data files are generated from the analytical phase functions derived in project 1. The data files are then used as input to a simulated SAR processor for either rectangular format or polar format signal processing. The simulation is useful for studying the effects of residual phase errors and for comparing the performance of different processing algorithms.

For example, Figure 1 shows the response of a spotlight mode SAR for two point targets processed with rectangular format recording. The center target is located at the reference position, and the response shown is the ideal response of a Kaiser window. The image of the second target is smeared (defocussed) and misplaced (misregistered). This example illustrates the serious degradation that results from using rectangular format processing in spotlight mode operation. Figure 2 shows the response that is obtained when ideal polar format recording is used. The reference target is again perfectly focussed, while the second target is only slightly degraded by residual phase errors. Figure 3 shows the system response when the polar-to-rectangular coordinate transformation is implemented with a 2D inverse distance (nonseparable) interpolation algorithm. This simulation shows that the smeared target can be recovered through correct processing, although there is evidence in Figure 3 of serious noise created

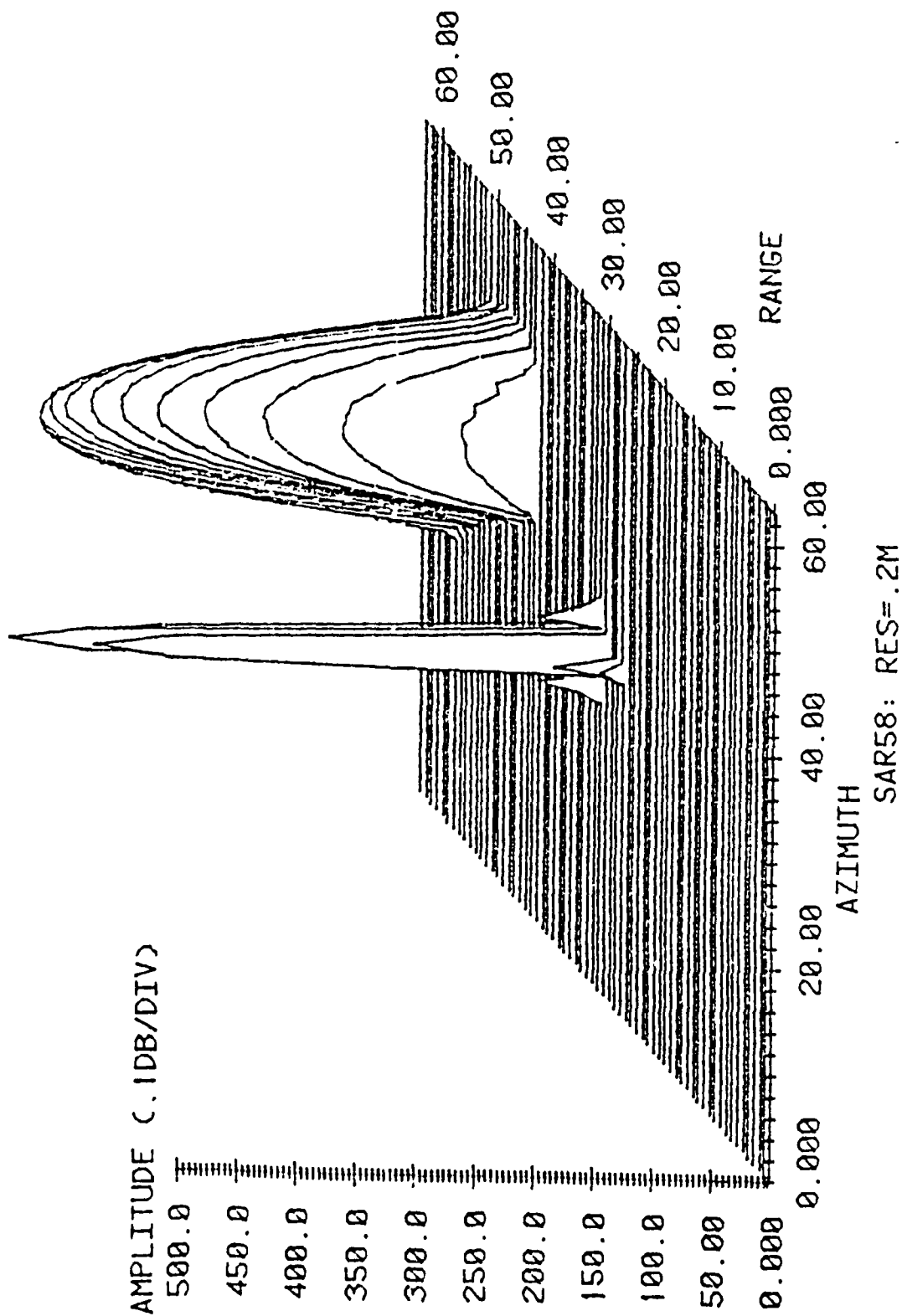
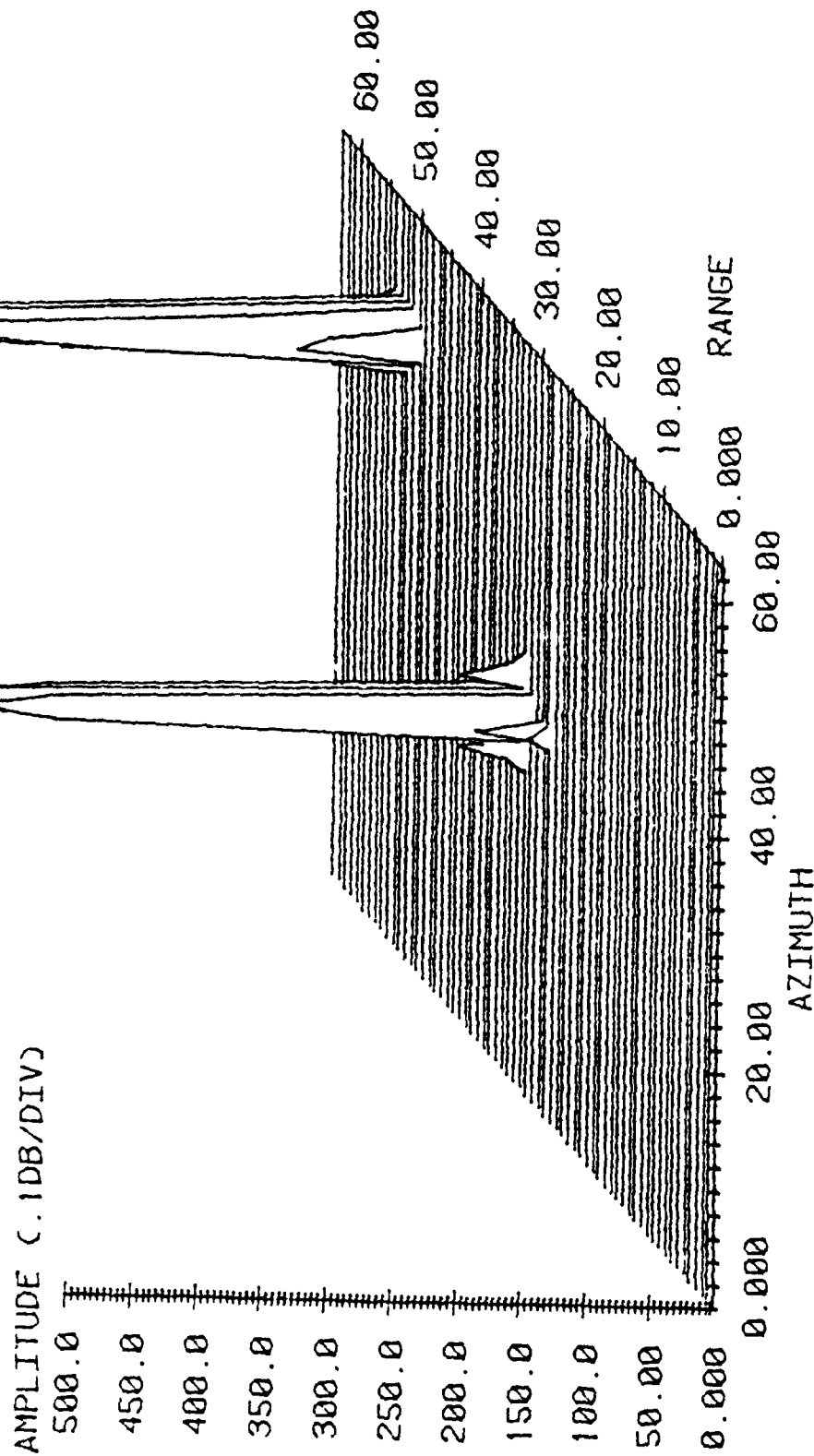


Figure 1 Simulation of point target response with rectangular format recording.



SAR72: RES=.2M

Figure 2 Simulation of point target response with ideal polar format recording (no interpolation error).

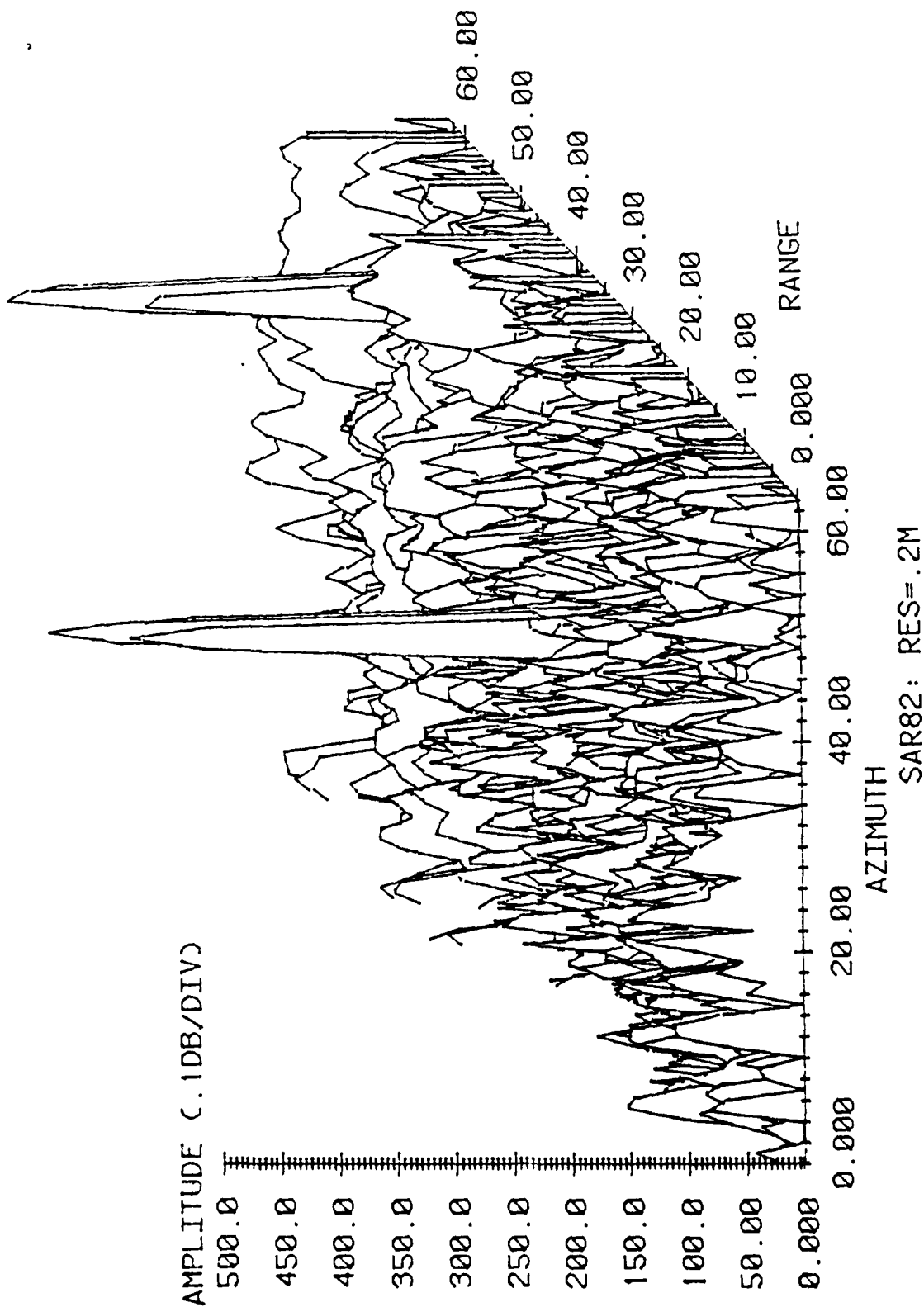


Figure 3 Simulation of point target response with polar format recording and 1st order nonseparable interpolation.

by the crude nature of the inverse interpolation algorithm. Simulation studies have investigated relationships between spread (defocus) and both target distance from the reference, and resolution [20].

1.3 Two-Dimensional Interpolators

In digital SAR processing 2D interpolation for polar-to-rectangular coordinate conversion is very complicated because the initial data points are non-uniformly spaced relative to the rectangular coordinate axes. Five types of 2D interpolators are presently under study: 1) 1st order inverse distance, 2) 1st order separable bilinear, 3) 3rd order separable Lagrange, 4) separable optimal FIR filtering, and 5) zero order interpolation with over-sampling. These simple interpolators have been selected because they have low computational complexities, although there are important questions to be answered regarding their quality of performance. Attempts are now in progress to characterize performance in terms of interpolation error. For example, Figures 4 and 5 show the frequency responses of the 1st order inverse distance and separable bilinear interpolators, respectively, as applied to uniformly spaced data samples. The energy in the sidelobes is lower for the separable bilinear filter, implying that this filter should result in better spacial domain performance. An important thrust of current work is to characterize performance through analytical techniques which represent the quality of the interpolator in terms of the sidelobe energy in the spectrum [19].

1.4 Residue Number Concepts for SAR Digital Processors

Research on this project involves an investigation of residue number concepts for realizing SAR digital processors with high speed capability and failure resistant behavior. This work is motivated because real-time SAR processing is severely demanding on the resources of a digital system, to the extent that dedicated processors are needed to satisfy data rate requirements. Residue number arithmetic has been known for many years for its potential for high speed addition and multiplication, although it has not been effective in general purpose computers because some functions, such as sign detection, magnitude comparison, and division are awkward and time consuming operators in the residue code. Within the last few years residue number arithmetic has captured the attention of researchers who are interested in digital signal processing (digital filtering, spectral analysis, decimation/interpolation, statistical analysis, etc.) rather than in the broader area of general purpose computing [11, 15].

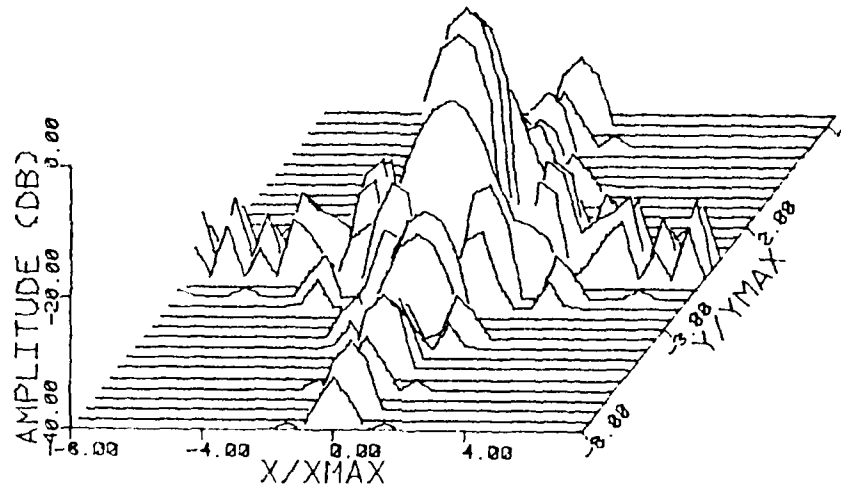


Figure 4 Frequency response of a 1st order nonseparable interpolator.

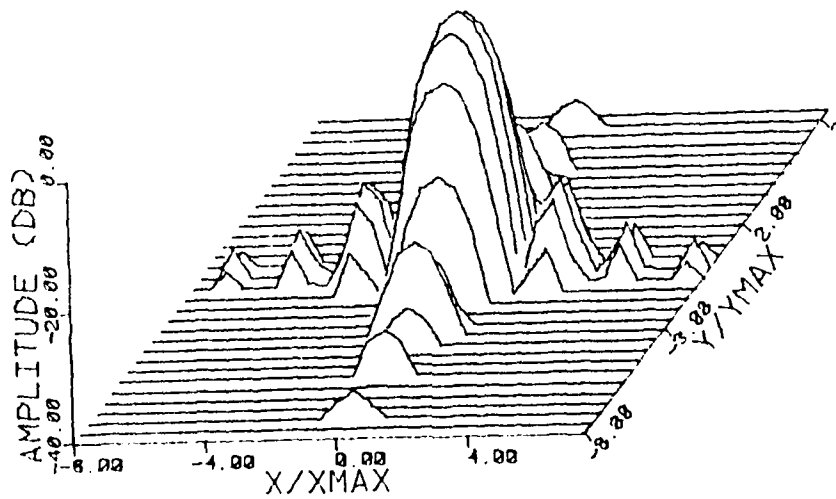


Figure 5 Frequency response of a 1st order separable interpolator.

In addition to high speed capabilities, residue number codes have a mathematical structure that facilitates error detection and correction when proper redundancy is added. These properties result from the parallel residue structure, (which prevents the propagation of errors) and the lack of a hierarchical significance among the digits, (which allows erroneous digits to be discarded without rendering the result completely useless). Our recent work at the Coordinated Science Laboratory has examined the theory of systematic redundant RNS coding for the isolation and detection of hardware failures, with subsequent "soft failure" that allows a faulty processor to continue operating with reduced capabilities [5, 7, 8, 14]. The theory is elegant and its capabilities are attractive in relation to the special requirements of SAR signal processing. One major concern at this time involves hardware complexity in the error checkers and the persistent question of reliability in the error checking hardware. One of the important thrusts of our present work is to determine desirable RNS structures and implementation techniques that can be realized in VLSI technology [5].

2. Future Directions

During our recent work in SAR several general observations have been made which provide motivation and direction for further research. The first is that it has become apparent to us that SAR processing is a specific case of a more general class of 2D digital array processing algorithms. The general class includes techniques used in computer-aided tomography, beam forming sonar, geophysical seismic processing, and radio astronomy. It is our belief that future SAR studies should include an evaluation and analysis of alternative 2D array algorithms used in these related areas. A second general observation is that many 2D array systems have one dimension that is inherently analog, and a second dimension that is inherently discrete. It is our belief that future studies should include hybrid signal processing techniques that will use both modern analog devices and sophisticated digital techniques to their maximum capabilities. Our third general observation is that failure resistance by means of residue number coding may be more efficiently realized by using the class of RNS product codes. Virtually all present work in redundant RNS signal processing has concentrated on the class of systematic RNS codes. There is some evidence that the product codes can lead to considerably less complexity in the error checkers, and therefore will be more useful in VLSI implementation of failure resistant processors.

3. Publications Supported by or Relating to Grant AFOSR-79-0029

- [1] G. Cortelazzo, "Frequency Domain Design of Multiband Finite Impulse Response Digital Filters Based on the Minimax Criterion," Master's Thesis, Department of Electrical Engineering, University of Illinois, Urbana-Champaign, IL, 1980.
- [2] G. Cortelazzo, M. R. Lightner, and W. K. Jenkins, "Frequency Domain Design of Multiband Finite Impulse Response Digital Filters Based on the Minimax Criterion," under review by the IEEE Trans. on Circuits and Systems, submitted September 1980.
- [3] G. Cortelazzo, M. R. Lightner, and W. K. Jenkins, "Frequency Domain Design of Multiband Finite Impulse Response Digital Filters Based on the Minimax Criterion," 1981 IEEE International Symposium on Circuits and Systems Proceedings, Chicago, IL, April 1981, to appear.
- [4] M. H. Etzel, "Residue Number System Recursive Digital Filtering with Error Correction Capabilities," Technical Report T-93, Coordinated Science Laboratory, University of Illinois, February 1980 (Ph.D. Dissertation).
- [5] M. H. Etzel and W. K. Jenkins, "Hardware Implementation of Failure Resistant Residue Number Digital Filters," 1981 International Symposium on Circuits and Systems Proceedings, Chicago, IL, April 1981, to appear.
- [6] M. H. Etzel and W. K. Jenkins, "The Design of Special Residue Classes for Efficient Recursive Digital Filter Realization," under review by the IEEE Trans. on Acoustics, Speech, and Signal Processing, submitted August 1979.
- [7] M. H. Etzel and W. K. Jenkins, "Redundant Residue Number Systems for Error Detection and Correction in Digital Filters," IEEE Trans. on Acoustics, Speech, and Signal Processing, Vol. ASSP-28, No. 5, October 1980, pp. 538-545.
- [8] M. H. Etzel and W. K. Jenkins, "Error Correction and Overflow Suppression Properties of RRNS Digital Filters," 1980 IEEE International Circuits and Systems Proceedings, Houston, TX, April 1980, pp. 1117-1120.

- [9] M. H. Etzel and W. K. Jenkins, "Digital Filters with Fault Tolerance," Proceedings of the 1979 Joint Automatic Control Conference, Denver, Co., June 1979, pp. 187-192.
- [10] S. A. Hirsch, "Software Implementation and Comparison of Two-Dimensional Finite Impulse Response Digital Filter Designs," Department of Electrical Engineering, University of Illinois, MS Thesis, 1980.
- [11] W. K. Jenkins, "Recent Advances in Residue Number Techniques for Recursive Digital Filtering," IEEE Trans. on Acoustics, Speech, and Signal Processing, Vol. ASSP-27, No. 1, February 1979, pp. 19-30.
- [12] W. K. Jenkins, "Complex Residue Number Arithmetic for High Speed Signal Processing," Electronics Letters, 14th August 1980, Vol. 16, No. 17, pp. 660-661.
- [13] W. K. Jenkins and M. H. Etzel, "Special Properties of Complement Codes for Redundant Residue Number Systems," Proc. IEEE, Vol. 69, No. 1, January 1981, pp. 132-133.
- [14] W. K. Jenkins, "Redundant Complex Residue Number Systems" Proceedings of the Very High Speed Computing Symposium, Georgia Institute of Technology, Atlanta, GA, September 1980, pp. IV.3-IV.20 (INVITED).
- [15] W. K. Jenkins, "The Effect of Algorithm Selection on the Performance of Monolithic Signal Processors," Proceedings of the 1980 National Electronics Conference, Chicago, IL, October 1980, pp. 425-430 (INVITED).
- [16] W. K. Jenkins, "Techniques in Digital Signal Signal Processing for Synthetic Aperture Radar," Proceedings of the 1979 International Symposium on Circuits and Systems, Tokyo, Japan, July 1979, pp. 979-980.
- [17] W. K. Jenkins, "Inherent Phase Distortion in Rectangular Format FFT Processing for Synthetic Aperture Radar," Proceedings of the Fourth International Symposium on Network Theory, Ljubljana, Yugoslavia, September 1979, pp. 101-105.

- [18] W. K. Jenkins and C. F. Lee, "Complex Residue Number Arithmetic for Digital Signal Processing," Proceedings of the 14th Asilomar Conference on Circuits, Systems, and Computers, Pacific Grove, CA, November 1980, to appear.
- [19] W. K. Jenkins, "Commonalities in Digital Array Processing for Synthetic Aperture Radar and Computer-Aided Tomography," manuscript in preparation, to be submitted to IEEE Trans. on Circuits and Systems, 1981.
- [20] D. A. Schwartz, "Analysis and Experimental Investigation of Three Synthetic Aperture Radar Formats," Technical Report T-94, Coordinated Science Laboratory, University of Illinois, February 1980.
- [21] R. G. Wolenty, "An Experimental Hardware Realization of a Multiple Microprocessor Residue Number Digital Filter," Master's Thesis, Department of Electrical Engineering, University of Illinois, Urbana-Champaign, IL 1979.
- [22] R. G. Wolenty and W. K. Jenkins, "An Experimental Hardware Realization of a multiple Microporcessor Residue Number Digital Filter," 1980 IEEE International Circuits and Systems Symposium Proceedings, Houston, TX, April 1980, pp. 1097-1100.

4. Related Research Grants and Submitted Proposals

<u>Agency</u>	<u>Grant Period</u>	<u>Yearly Funding</u> (approximate)	<u>Status</u>
NSF	7/15/79-7/14/81	\$25,000	(Active)
ARO	2/1/81- /31/83	45,000	(In Review)
AFOSR	5/1/81-4/30/83	60,000	(In Review)
JSEP	4/1/81-9/31/83	25,000	(Approved)

DATE
FILMED
-8